Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-12 (cancelled)

Claim 13. (currently amended) ~~The non volatile memory of claim 8 wherein,~~ A non volatile memory, comprising:

a) flash memory cells organized in rows and columns,

b) cells in a row are interconnected by a word line connecting to control gates of said flash memory cells in said row,

c) cell layout in a column mirrors cell layout in adjacent columns producing a first pair of adjacent columns with drains close together and a second pair of adjacent columns with sources close together,

d) a bit line extends full length of said columns, laying between said first pair of adjacent columns and connecting said drains of said first pair of adjacent columns to a sense amplifier,

e) a source line extends full length of said columns, laying between said second pair of adjacent columns and connecting said sources of said second pair of adjacent columns to source voltages,

f) a program operation of said flash memory cells organized by a vertical page associated with said source line whereby a source line voltage and a bit line voltage of said vertical page are set for said program operation and a word line program voltage is stepped from cell to cell,

g) an erase operation of said flash memory cells organized by horizontal block whereby all bit lines, source lines and word lines are coupled to a same voltage and then word lines coupled to cells to be erased are biased to an erase voltage.

h) said cell layout in a column is a same said cell layout in adjacent columns producing a first adjacent column with drains of cells connected to a first source line and sources of cells connected to a first bit line, and a second adjacent column with sources of cells connected to said first source line and drains of cells in said second adjacent column connected to a second bit line, allowing vertical page programming and horizontal page/block erase.

14. (previously presented) The non volatile memory of claim 13 wherein, bit lines extend full length of said columns, laying between a first pair of adjacent columns, connecting to said drains of a first column of said first pair of adjacent columns, to said sources of a second column of said first pair of adjacent columns, and connecting to a sense amplifier when performing a read operation.

15. (previously presented) The non volatile memory of claim 13 wherein, source lines extend full length of said columns, laying between a second pair of adjacent

columns, connecting to said sources of a first column of said second pair of adjacent columns, connecting to said drains of said second pair of adjacent columns, and connecting to source voltages.

Claims 16-25 (canceled)